MICROELECTRONIC DEVICES AND METHODS FOR FILLING VIAS IN MICROELECTRONIC DEVICES

APPLICATION(S) INCORPORATED BY REFERENCE

[0001] This application is related to U.S. Patent Application No. (Attorney Docket No. 10829.8742US00; Micron Disclosure Nos. 03-0599 and 03-0613) entitled MICROELECTRONIC DEVICES, METHODS FOR FORMING VIAS IN MICROELECTRONIC DEVICES, AND METHODS FOR PACKAGING MICROELECTRONIC DEVICES, filed concurrently herewith and incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] The following disclosure relates generally to microelectronic devices and, more particularly, to methods for filling vias in microelectronic workpieces.

BACKGROUND

[0003] Conventional packaged microelectronic devices can include a singulated microelectronic die, an interposer substrate or lead frame attached to the die, and a moulded casing around the die. The die generally includes an integrated circuit and a plurality of bond-pads coupled to the integrated circuit. The bond-pads are typically coupled to terminals on the interposer substrate or lead frame, and serve as external electrical contacts on the die through which supply voltage, signals, etc., are transmitted to and from the integrated circuit. In addition to the terminals, the interposer substrate can also include ball-pads coupled to the terminals by conductive traces supported in a dielectric material. Solder balls can be attached to the ball-pads in one-to-one correspondence to define a "ball-grid array."

Packaged microelectronic devices with ball-grid arrays are generally higher grade packages having lower profiles and higher pin counts than conventional packages using lead frames.

[0004] Packaging processes for conventional microelectronic devices typically include (a) cutting the wafer to separate or singulate the dies, (b) attaching the individual dies to an interposer substrate, (c) wire-bonding the bond-pads of the dies to the terminals of the interposer substrate, and (d) encapsulating the dies with a suitable molding compound. One challenge of conventional packaging processes is that mounting the individual dies to interposer substrates or lead frames is time-consuming and expensive. Another challenge is forming wire-bonds that can withstand the forces of the molding compound during encapsulation; this issue is particularly problematic as the wire-bonds become smaller to accommodate higher pin counts and smaller packages. Yet another challenge of conventional packaging processes is that attaching individual dies to interposer substrates or lead frames may damage the bare dies. As such, processes for packaging the dies has become a significant factor in manufacturing microelectronic devices.

[0005] Another process for packaging microelectronic devices is wafer-level packaging. In this process, a plurality of microelectronic dies are formed on a wafer, and then a redistribution layer is formed over the dies. The redistribution layer can include a dielectric layer and a plurality of exposed ball-pads forming arrays on the dielectric layer. Each ball-pad array is typically arranged over a corresponding die, and the ball-pads in each array are coupled to corresponding bond-pads of the die by conductive traces extending through the dielectric layer. After forming the redistribution layer on the wafer, discrete masses of solder paste are deposited onto the individual ball-pads. The solder paste is then reflowed to form small solder balls or "solder bumps" on the ball-pads. After forming the solder balls, the wafer is singulated to separate the individual microelectronic devices from each other.

[0006] Wafer-level packaging is a promising development for increasing efficiency and reducing the cost of microelectronic devices. By "pre-packaging" individual dies with a redistribution layer before cutting the wafers to singulate the dies, sophisticated semiconductor processing techniques can be used to form smaller arrays of solder balls. Additionally, wafer-level packaging is an efficient process that simultaneously packages a plurality of dies, thereby reducing costs and increasing throughput.

[0007] Packaged microelectronic devices such as those described above are used in cellphones, pagers, personal digital assistants, computers, and many other electronic products. To meet the demand for smaller electronic products, there is a continuing drive to increase the performance of packaged microelectronic devices, while at the same time reducing the height and the surface area or "footprint" of such devices on printed circuit boards. Reducing the size of high performance devices, however, is difficult because the sophisticated integrated circuitry requires more bond-pads, which results in larger ball-grid arrays and thus larger footprints. One technique for increasing the component density of microelectronic devices within a given footprint is to stack one device on top of another.

[0008] Figure 1 schematically illustrates a first microelectronic device 10 attached to a second microelectronic device 20 in a wire-bonded, stacked-die arrangement. The first microelectronic device 10 includes a die 12 having an integrated circuit 14 electrically coupled to a series of bond-pads 16. A redistribution layer 18 electrically couples a plurality of first solder balls 11 to corresponding bond-pads 16. The second microelectronic device 20 similarly includes a die 22 having an integrated circuit 24 electrically coupled to a series of bond-pads 26. A redistribution layer 28 electrically couples a plurality of second solder balls 21 to corresponding bond-pads 26. Wire-bonds 13 extending from the first solder balls 11 to the second solder balls 21 electrically couple the first microelectronic device 10 to the second microelectronic device 20.

[0009] The second solder balls 21 on the second microelectronic device 20 are positioned outboard of the first microelectronic device 10 to facilitate installation of the wire-bonds 13. Positioning the second solder balls 21 in this manner undesirably increases the footprint of the stacked-die arrangement. In addition, installation of the wire-bonds 13 can be a complex and/or expensive process because it requires placing individual wires between each pair of solder balls. Further, this type of installation may not be feasible for the high-density, fine-pitch arrays of some high-performance devices because the solder balls are not spaced apart far enough to be connected to individual wire-bonds.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 schematically illustrates a first microelectronic device attached to a second microelectronic device in a stacked-die arrangement in accordance with the prior art.

[0011] Figure 2 is a cut-away isometric view of a microfeature workpiece configured in accordance with an embodiment of the invention.

[0012] Figure 3 is a schematic cross-sectional view of the microfeature workpiece of Figure 2 taken substantially along line 3-3 in Figure 2.

[0013] Figure 4 is a schematic cross-sectional view illustrating a method of forming a conductive interconnect in a microelectronic device in accordance with an embodiment of the invention.

[0014] Figures 5A-5B are schematic cross-sectional views illustrating various stages in a method of forming a conductive interconnect in a microelectronic device in accordance with another embodiment of the invention.

[0015] Figures 6A-6D are schematic cross-sectional views illustrating various stages in a method of forming a conductive interconnect in a microelectronic device in accordance with a further embodiment of the invention.

[0016] Figures 7A-7B are schematic cross-sectional views illustrating various stages in a method of forming a conductive interconnect in a microelectronic device in accordance with yet another embodiment of the invention.

[0017] Figures 7C-7D are schematic cross-sectional views illustrating various stages in a method of forming a bond-pad electrically coupled to the conductive interconnect of Figure 7B.

[0018] Figure 8 is a schematic cross-sectional view illustrating a method of forming a conductive interconnect in a microelectronic device using solder tent technology in accordance with a further embodiment of the invention.

DETAILED DESCRIPTION

A. Overview

[0019] The following disclosure describes several embodiments of microelectronic devices, methods for packaging microelectronic devices, and methods for filling vias in dies and other substrates to form conductive interconnects. One aspect of the invention is directed toward a method of forming a conductive interconnect in a microelectronic device. In one embodiment, the method includes providing a microfeature workpiece having a plurality of dies and at least one passage extending through the microfeature workpiece from a first side of the microfeature workpiece to an opposite second side of the microfeature workpiece. The method can further include forming a conductive plug in the passage adjacent to the first side of the microelectronic workpiece. A conductive material is then deposited in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece.

[0020] In one aspect of this embodiment, forming a conductive plug in the passage can include depositing an electrically conductive material in the passage using a maskless mesoscale materials deposition process. In another embodiment, forming the conductive plug can include applying an electronic ink in the passage using an electronic printing process. In a further embodiment, forming the conductive plug can include depositing an electrically conductive material in the passage using a nano-particle deposition process.

[0021] A further aspect of the invention is directed toward another method of forming a conductive interconnect in a microelectronic device. In one

embodiment, this method includes providing a microfeature workpiece having a plurality of dies and at least one passage extending through the microfeature workpiece from a first side of the microfeature workpiece to an opposite second side of the microfeature workpiece. The passage can define a first opening in the first side of the microfeature workpiece and a second opening in the second side of the microfeature workpiece. The method can further include applying a sealing layer to the first side of the microfeature workpiece to at least generally seal the first opening of the passage. A first portion of conductive material can then be deposited through the second opening of the passage to form a plug in the passage adjacent to the sealing layer. After the plug has been formed, a second portion of conductive material can be deposited through the second opening of the passage to at least generally fill the passage from the plug to the second side of the microelectronic workpiece.

[0022] Many specific details of the present invention are described below with reference to semiconductor devices. The term "microfeature workpiece," however, as used throughout this disclosure includes substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, read/write components, and other features are fabricated. For example, such microelectronic workpieces can include semiconductor wafers (e.g., silicon or gallium arsenide wafers), glass substrates, insulated substrates, and many other types of substrates. The feature signs in microfeature workpieces can include very small features of 0.11 μm or less, but larger features are also included on microfeature workpieces.

[0023] Specific details of several embodiments of the invention are described below with reference to microelectronic dies and other microelectronic devices in order to provide a thorough understanding of such embodiments. Other details describing well-known structures often associated with microelectronic devices are not set forth in the following description to avoid unnecessarily obscuring the description of the various embodiments. Persons of ordinary skill in the art will understand, however, that the invention may have other embodiments with

additional elements or without several of the elements shown and described below with reference to Figures 2-8.

[0024] In the Figures, identical reference numbers identify identical or at least generally similar elements. To facilitate the discussion of any particular element, the most significant digit or digits of any reference number refer to the Figure in which that element is first introduced. For example, element 210 is first introduced and discussed with reference to Figure 2.

B. Embodiments of Microfeature Workpieces

[0025] Figure 2 is a cut-away isometric view of a wafer or microfeature workpiece 200 configured in accordance with an embodiment of the invention. In one aspect of this embodiment, the microfeature workpiece 200 includes a front side 201, a back side 202, and a plurality of microelectronic devices 210 (identified individually as microelectronic devices 210a-f). Each microelectronic device 210 can include a microelectronic die 212 having an integrated circuit 214 (shown schematically), and a plurality of metallic and/or conductive bond-pads 216 electrically coupled to the integrated circuit 214. The microfeature workpiece 200 can further include a passivation layer 240 covering the front side 201 of the die 212 except for openings 218 at each of the bond-pads 216.

[0026] In the embodiment illustrated in Figure 2, the processing of the microelectronic devices 210 has not been completed. As described below with reference to Figures 3-7B, additional processing can be carried out on the microfeature workpiece 200 to configure or package the individual microelectronic devices 210 for use in an electronic device or product. After this additional processing is complete, the microfeature workpiece 200 can be cut along lines A_1-A_1 to singulate the microelectronic devices 210.

[0027] Figure 3 is a schematic cross-sectional view of the microelectronic device 210b taken substantially along line 3-3 in Figure 2 in accordance with an embodiment of the invention. The microelectronic device 210b is inverted in Figure 3 for purposes of illustration, and it has undergone additional processing beyond that illustrated in Figure 2. For example, in one aspect of this

embodiment, the microelectronic device 210b includes a via or passage 342 extending through the die 212 and the bond-pad 216. The passage 342 and the opening 218 define a first opening 346 in the front side 201 of the microfeature workpiece 200, and a second opening 348 in the back side 202. In one embodiment, the passage 342 can be formed using a laser-cutting method at least generally similar to one or more of the methods described in co-pending U.S. Patent Application No. (Attorney Docket No. 10829.8742US00), entitled MICROELECTRONIC DEVICES, METHODS FOR FORMING VIAS IN MICROELECTRONIC DEVICES, AND METHODS FOR PACKAGING MICROELECTRONIC DEVICES. In other embodiments, the passage 342 can be formed using other methods, such as a suitable etching or drilling method. Although, in one embodiment, the passage 342 may be slightly tapered as depicted in Figure 3, in other embodiments, the passage 342 can be straight or at least approximately straight.

[0028] After the passage 342 has been formed, a dielectric layer 344 can be applied to the inner wall of the passage 342. In one embodiment, the dielectric layer 344 is an oxide applied in a low temperature chemical vapor deposition (CVD) process. In other embodiments, the dielectric layer 344 is a polyamide material or other materials suitable for insulating the die 212 from electrical leakage after the passage 342 has been filled with conductive metal (not shown) as described in greater detail below.

[0029] Figure 4 is a schematic cross-sectional view illustrating a method of forming a conductive interconnect in the microelectronic device 210b of Figure 3 in accordance with an embodiment of the invention. In one aspect of this embodiment, a conductive element 450 is positioned against the passivation layer 240 so that a contact surface 451 at least generally covers the first opening 346 of the passage 342. Once the conductive element 450 is in this position, the passage 342 can be filled with conductive material 445 to form a conductive interconnect 446 extending through the microelectronic device 210b. For example, in one embodiment, the conductive element 450 is a conductive polymer

that can be biased at an electrical potential to electroplate the conductive material 445 in the passage 342. The conductive material 445 can be copper or other conductive metals, such as silver, gold, palladium, etc. In still further embodiments, other conductive materials that can be deposited at low temperatures of 250°C or less to fill the passage 342.

[0030] One shortcoming associated with the method described above with reference to Figure 4 is that occasionally the conductive element 450 allows some of the conductive material 445 to leak out of the first opening 346 and flow between the contact surface 451 and the passivation layer 240. This leaked material can extend between two or more bond-pads 216 (Figure 2) and cause undesirable shorting between the bond-pads 216.

[0031] Figures 5A-5B are schematic cross-sectional views illustrating various stages in a method of forming a conductive interconnect in the microelectronic device 210b of Figure 3 in accordance with another embodiment of the invention. Referring first to Figure 5A, this method starts with the microelectronic device 210b configured as shown in Figure 3. From there, a conductive plug 560 is formed in the passage 342 adjacent to the bond-pad 216. The conductive plug 560 can be formed with conductive material that fills a portion of the passage 342 and electrically couples to an exposed surface of the bond-pad 216 that is not insulated by the dielectric layer 344. In one embodiment, the conductive plug 560 can be formed by depositing an electrically conductive material in the passage 342 using a maskless mesoscale materials deposition process. One such process includes the M^3D technology offered by Optomec, Inc., of 3911 Singer Boulevard NE, Albuquerque, NM 87109. In other embodiments, the conductive plug 560 can be formed using other suitable methods. For example, in one other embodiment, the conductive plug 560 can include an electronic ink applied to the passage 342 using an electronic printing process. In yet other embodiments, the conductive plug 560 can be formed by depositing electrically conductive material in the passage 342 using a nano-particle deposition process. In any of the foregoing embodiments, the conductive plug 560 can include silver. In other

embodiments, the conductive plug 560 can include other electrically conductive materials, such as gold, copper, palladium and/or various solders. Such materials can include those that can be deposited and/or printed in a conductive ink or paste at a low temperature, such as 250° C or less.

[0032] Referring next to Figure 5B, after the conductive plug 560 is in place, the remaining portion of the passage 342 can be filled with a conductive material 545 to form a conductive interconnect 546 extending through the microelectronic device 210b. For example, in one embodiment the conductive plug 560 can serve as an electrode for electroplating the passage 342 with a suitable material, such as copper. In this embodiment, a conductive element 550 is positioned against the conductive plug 560 and biased at an electrical potential to electroplate the conductive material 545 within the passage 342. In other embodiments, other methods can be used to bias the conductive plug 560 at an electrical potential suitable for electroplating material into the passage 342.

[0033] Figures 6A-6D are schematic cross-sectional views illustrating various stages in a method of forming a conductive interconnect in a microelectronic device 610 in accordance with an embodiment of the invention. Referring first to Figure 6A, the microelectronic device 610 can include a die 612 having a through-hole or passage 642. The passage 642 defines a first opening 636 in a first side 601 of the microelectronic device 610 and a second opening 638 in a second side 602. A passivation layer 644 covers the die 612 including the inner wall of the passage 642. In one embodiment, the passivation layer 644 can be tetraethylorthosilicate (TEOS) deposited using a low temperature CVD process. In other embodiments, the passivation layer 644 can be parylene and/or other suitable materials, such as silicon dioxide (SiO_2) or silicon nitrite (Si_3N_4). The foregoing list of passivation and/or dielectric material options is not exhaustive. Accordingly, in other embodiments, it is expected that other suitable materials and processes can be used to form one or more of the passivation and/or dielectric layers discussed herein.

[0034] Referring next to Figure 6B, a tape, film, or other type of suitable sealing layer 670 can be temporarily applied to the die 612 to at least generally seal the first opening 636 of the passage 642. After the first opening 636 has been sealed, a first portion of conductive material is deposited through the second opening 638 to form a plug 660 in the passage 642 adjacent to the sealing layer 670. In one embodiment, forming the plug 660 can include depositing an electrically conductive material in the passage using a maskless mesoscale materials deposition process as described above with reference to Figure 5A. In another embodiment, forming the plug 660 can include applying an electronic ink in the passage 642 using an electronic printing process. In yet another embodiment, forming the plug 660 can include depositing an electrically conductive material in the passage 642 using a nano-particle deposition process to deposit silver or other suitable metal.

[0035] As shown in Figure 6C, the sealing layer 670 (Figure 6B) is removed from the microelectronic device 610, and a conductive element 650 is positioned against the microelectronic device 610 so that a contact surface 651 makes electrical contact with the plug 660. As described above with reference to the embodiments shown in Figures 4 and 5B, the conductive element 650 can include an electrode configured to bias the plug 660 at an electrical potential for electroplating the passage 642 with a second portion of conductive material 645 to form a conductive interconnect 646 extending through the microelectronic device 610.

[0036] Referring to Figure 6D, after the conductive interconnect 646 has been formed, additional processing steps can be carried out to package the microelectronic device 610 for use in a microelectronic device set. Such a microelectronic set can include a set having a stacked-die arrangement. In one embodiment, such processing steps can include removing the passivation layer 644 (Figure 6A) from a first surface 631 of the die 612, and forming a bond-pad 616 on the die 612 electrically coupled to the conductive interconnect 646. In other embodiments, other processing steps can be employed to configure the

microelectronic device 610 in a suitable form for subsequent use in a microelectronic device set or product.

[0037] Figures 7A-7B are schematic cross-sectional views illustrating various stages in a method of forming a conductive interconnect in the microelectronic device 610 in accordance with an embodiment of the invention that is similar to the embodiment described above with reference to Figures 6A-6D. In one aspect of this embodiment as shown in Figure 7A, after the plug 660 is formed in the passage 642, the sealing layer 670 (Figure 6B) is removed and a metallic layer 780 is deposited on the passivation layer 644 in electrical contact with the plug 660. In one embodiment, the metallic layer 780 can be a metal layer formed by physical vapor deposition (PVD). In other embodiments, the metallic layer 780 can include other materials formed by other processes, such as a suitable CVD process.

[0038] Referring next to Figure 7B, after the metallic layer 780 has been deposited on the microelectronic device 610, the conductive element 650 is positioned against the metallic layer 780. As discussed above, the conductive element 650 can be a plate electrode or a conductive polymer configured to apply an electrical bias to the metallic layer 780, which in turn biases the plug 660. The conductive element 650, however, can be a finger type contact as shown in U.S. Application No. 6,080,291, which is herein incorporated by reference. Electrically biasing the plug 660 facilitates electroplating a second portion of conductive material 745 in the passage 642 adjacent to the plug 660. Together, the plug 660 and the second portion of conductive material 745 form a conductive interconnect 746 extending through the microelectronic device 610.

[0039] Figures 7C-7D are schematic cross-sectional views illustrating various stages in a method of forming a bond-pad electrically coupled to the plug 660 in accordance with an embodiment of the invention. In one aspect of this embodiment as shown in Figure 7C, a resist layer 790 is formed on the metallic layer 780, and an opening 718 is formed in the resist layer 790 adjacent to the plug 660. A metallic portion 792 is then deposited on the metallic layer 780

through the opening 718 by using the metallic layer 780 as a seed layer. After depositing the metallic portion 792, the resist layer 790 is removed as shown in Figure 7D. In addition, all of the metallic layer 780, except for the portion under the metallic portion 792, is also removed (for example, by a suitable etching process). Together, the remaining metallic layer 780 and metallic portion 792 form a bond-pad 716 electrically coupled to the plug 660. Although the foregoing discussion describes one method for forming a bond-pad on the microelectronic device 610, in other embodiments, other methods can be used to form bond-pads electrically coupled to the plug 660.

[0040] Figure 8 is a schematic cross-sectional view illustrating a method of forming a conductive interconnect in the microelectronic device 210b of Figure 3 using solder tent technology in accordance with a further embodiment of the invention. This method starts with the microelectronic device 210b configured as shown in Figure 3. From there, a metallic material 868 is applied to the bond pad 216 by plating or another suitable process. In one aspect of this embodiment, the bond pad 216 can be Aluminum (Al) and the metallic material 868 can be Nickel (Ni) that acts as a wetting agent to help subsequent material applications adhere to the bond pad 216. After the metallic material 868 has been applied, a conductive plug 860 is formed to fill a portion of the passage 342 and electrically couple to the bond-pad 216. In one embodiment, the conductive plug 860 can be formed by depositing an electrically conductive material in the passage 342 using solder tent technology. In this embodiment, the conductive plug can include Tin-Lead (SnPb), Tin-Silver-Copper (SnAgCu), Tin-Cu (SnCu), or Tin-Silver (SnAg) material, among others. After the conductive plug 860 is in place, the remaining portion of the passage 342 can be filled with a conductive material using one or more of the methods described above (such as the method described above with reference to Figure 5B) to form a conductive interconnect 846 extending through the microelectronic device 210b.

[0041] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various

modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.